One Technology Way • P.O. Box 9106 • Norwood, MA 02062-9106, U.S.A. • Tel: 781.329.4700 • Fax: 781.461.3113 • www.analog.com

Evaluating the ADMV1014 24.5 GHz to 43.5 GHz, Wideband Downconverter

FEATURES

Full featured evaluation board for the ADMV1014
On-board USB for SPI control
5 V operation
ACE software interface for SPI control

EVALUATION KIT CONTENTS

ADMV1014-EVALZ evaluation board

EQUIPMENT NEEDED

5 V dc power supply
RF signal generator
Spectrum analyzer

DOCUMENTS NEEDED

ADMV1014 data sheet
ADMV1014-EVALZ evaluation board user guide

SOFTWARE NEEDED

ACE software
USB drivers for the ADMV1014-045188, Rev. A (ADMV1014-EVALZ) evaluation board

GENERAL DESCRIPTION

The ADMV1014 is a silicon germanium (SiGe) design, wideband, microwave downconverter optimized for point to point microwave radio designs operating in the 24.5 GHz to 43.5 GHz frequency range.

The downconverter offers two modes of frequency translation. The device is capable of direct quadrature demodulation to baseband I/Q output signals, as well as image rejection downconversion to a complex intermediate frequency (IF) output carrier frequency. The baseband outputs can be dc-coupled, but are typically ac-coupled with a sufficiently low, high pass corner frequency to ensure adequate demodulation accuracy. The serial port interface (SPI) allows fine adjustment of the quadrature phase to allow the user to optimize I/Q demodulation performance. Alternatively, the baseband I/Q outputs can be disabled, and the I/Q signals can be passed through an on-chip active balun to provide two single-ended, quadrature, complex IF outputs between 800 MHz and 6000 MHz. When used as an image rejecting downconverter, the unwanted image term is typically suppressed to better than 30 dBc below the desired sideband. The ADMV1014 offers a flexible local oscillator (LO) system, including a frequency quadruple option allowing a range of LO frequencies from 21.6 GHz to 41 GHz to cover a radio frequency (RF) input range as wide as 24.5 GHz to 44 GHz. A square law power detector is provided to allow monitoring of the power levels at the mixer inputs. The detector output can be used to provide closed-loop control of the RF input variable attenuator through an external op-amp error integrator circuit.

The ADMV1014 downconverter comes in a compact, thermally enhanced, 5 mm × 5 mm flip chip CSP package. The ADMV1014 operates over the −40°C to +85°C case temperature range.

The ADMV1014-EVALZ evaluation board incorporates the ADMV1014 with a microcontroller, low dropout (LDO) regulators, and *nano*DAC® to allow quick and easy evaluation of the ADMV1014. The microcontroller allows the user to configure the ADMV1014 register map through the Analysis, Control, Evaluation (ACE) software. The LDO regulators allow the ADMV1014 to be powered on by a single supply and offer optimal power supply ripple rejection. The *nano*DAC allows the user to attenuate the RF power going into the mixer of ADMV1014 without using an external power supply.

For full details on the ADMV1014, see the ADMV1014 data sheet, which must be consulted in conjunction with this user guide when using the ADMV1014-EVALZ evaluation board.

TABLE OF CONTENTS

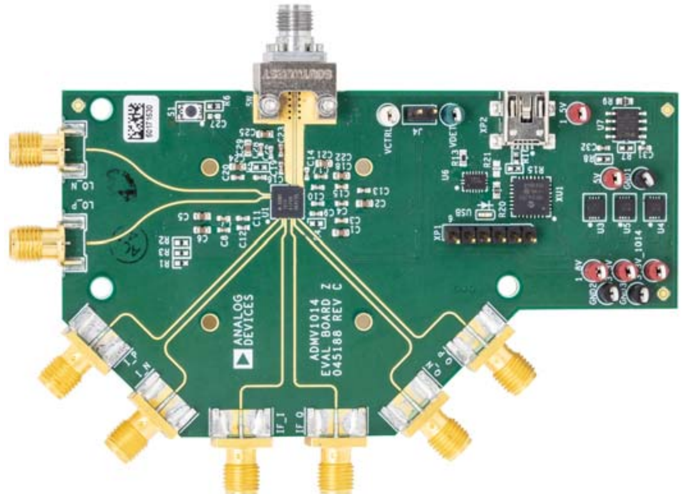
REVISION HISTORY

4/2019—Rev. 0 to Rev. A

Changes to Evaluation Board Hardware Section, Figure 2, and Figure 4 ... 4
Changes to Figure 6 ... 5
Changes to Figure 7 ... 6
Changes to Installing the ACE Software and ADMV1014 Plugins and Drivers Section ... 7
Changes to Initial Setup Section ... 8
Added Updating Register 0x0B Sequence Section ... 12
Changes to Figure 19 ... 14
Changes to Figure 22 and Figure 24 ... 16

10/2018—Revision 0: Initial Version

EVALUATION BOARD PHOTOGRAPH



17173-001

Figure 1.

EVALUATION BOARD HARDWARE

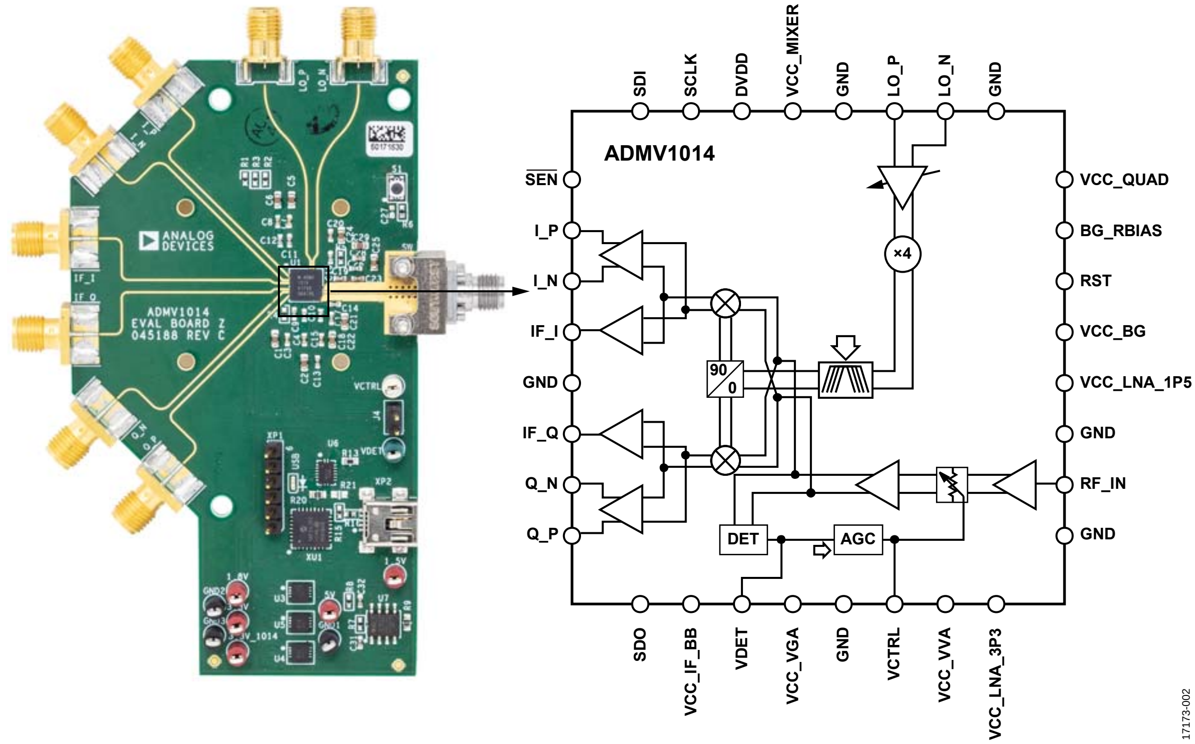


Figure 2. Evaluation Board Configuration

The ADMV1014-EVALZ evaluation board comes with an ADMV1014 chip. Figure 2 shows the location of this chip on the ADMV1014-EVALZ evaluation board and the block diagram of the ADMV1014.

The LO input path operates from 5.4 GHz to 10.25 GHz with an LO amplitude range of −6 dBm to +6 dBm. The LO input path also has an internal quadrupler (×4) and programmable band-pass filter. Program the LO band-pass filter from Register 0x04, QUAD_FILTERS (Register 0x09, Bits[3:0]).

The LO path operates in either differential or single-ended mode. LO_P and LO_N are the inputs to the LO path. Switch the LO path from differential to single-ended by setting the QUAD_SE_MODE bits (Register 0x04, Bits[9:6]).

Figure 3 shows a block diagram of the LO path.

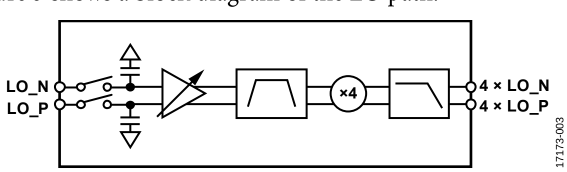


Figure 3. LO Path Block Diagram

The ADMV1014-EVALZ evaluation board has IF outputs (IF_I and IF_Q) for single sideband downconversion, and I/Q outputs (I_P, I_N, Q_P, and Q_N) for direct conversion for RF to I/Q. When evaluating the device in IF mode, connect the IF outputs through a 90° hybrid to a spectrum analyzer. When using IF mode, the I/Q outputs are floating. When evaluating the devices in I/Q mode, connect the I/Q outputs (I_P, I_N, Q_P, and Q_N) to an I/Q baseband analyzer. The ADMV1014-EVALZ evaluation board runs on a 5 V dc supply. Figure 4 shows the top side of the ADMV1014-EVALZ evaluation board and is intended for evaluation purposes only with no implied guarantee of performance or reliability.

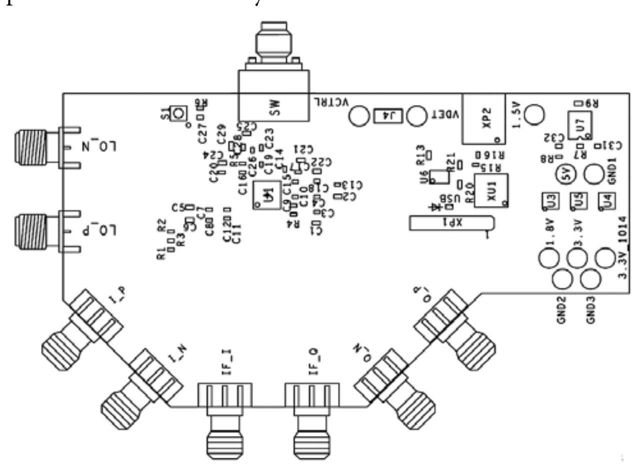


Figure 4. Top View of the ADMV1014-EVALZ

Connect the 5 V dc connection to the 5 V test point, and connect the ground connection to the GND1 test point. The 3.3 V, 1.8 V, and 1.5 V test points are for evaluation purposes only. Connect the signal generator to the Southwest/SRI 2.92 mm connector, RFIN. Connect LO_N and LO_P, the Southwest/SRI 2.92 mm connectors, differentially to the low phase noise signal generator. Use a 180° hybrid for the differential inputs. In IF mode, connect IF_I and IF_Q to the spectrum analyzer (use a 90° hybrid) and keep the I/Q outputs floating. In I/Q mode, connect I_P, I_N, Q_N, and Q_P to the I/Q baseband analyzer and keep the IF_I and IF_Q floating. Use the mini USB connector (XP2) to connect the PC to the ADMV1014-EVALZ evaluation board. Before using the SPI, press the S1 button to hard reset the ADMV1014.

See Figure 6 and Figure 7 for the ADMV1014-EVALZ lab connections. Use the AD5601 *nano*DAC® to generate the VCTRL voltage (see the Setting VCTRL Voltage for the ADMV1014 section for additional details). Figure 5 shows the block diagram of the ADMV1014 lab bench setup. Figure 4 shows the top view of the ADMV1014-EVALZ. The ADMV1014-EVALZ also features a reset button to hard reset the ADMV1014-EVALZ.

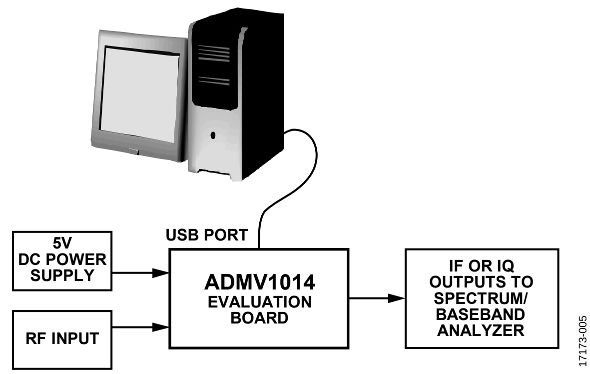


Figure 5. Block Diagram of the ADMV1014

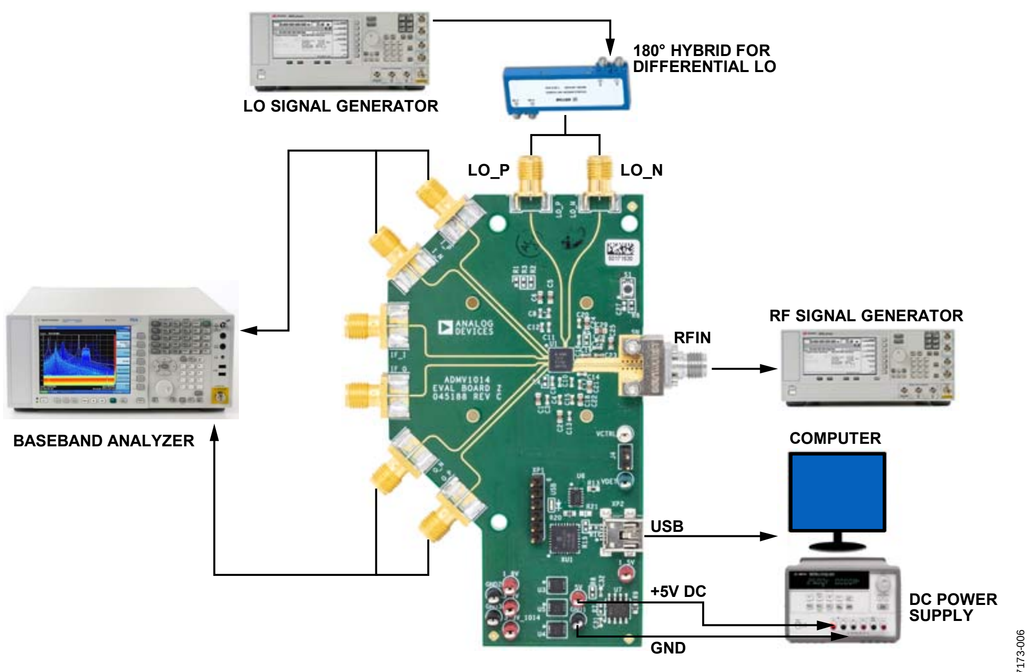


Figure 6. ADMV1014 Lab Bench Setup for I/Q Mode

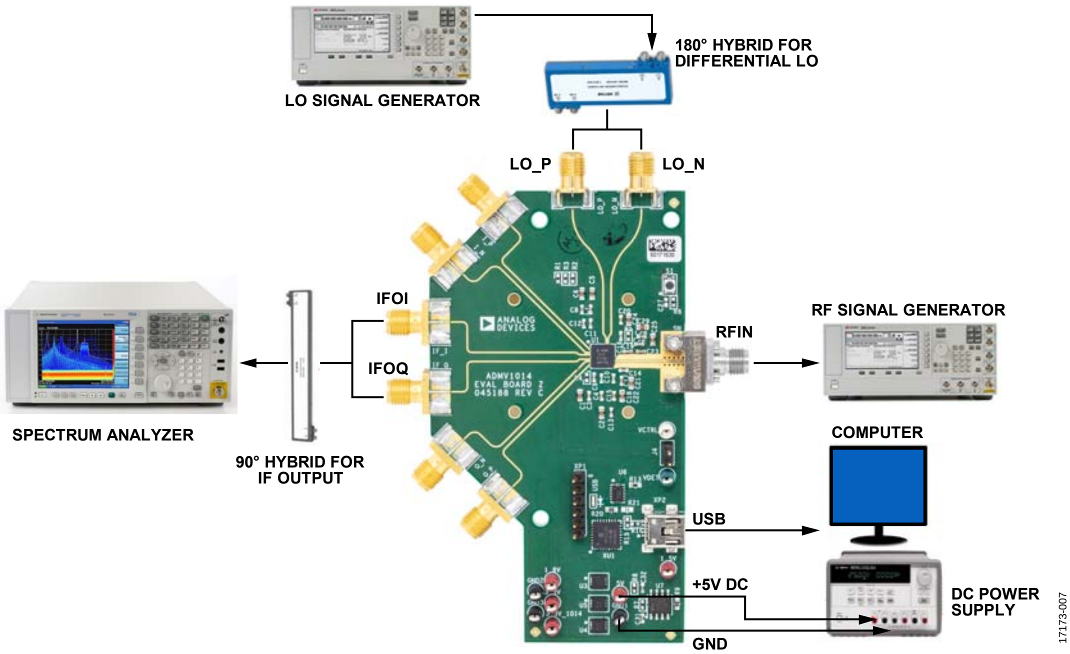


Figure 7. ADMV1014 Lab Bench Setup for IF Mode

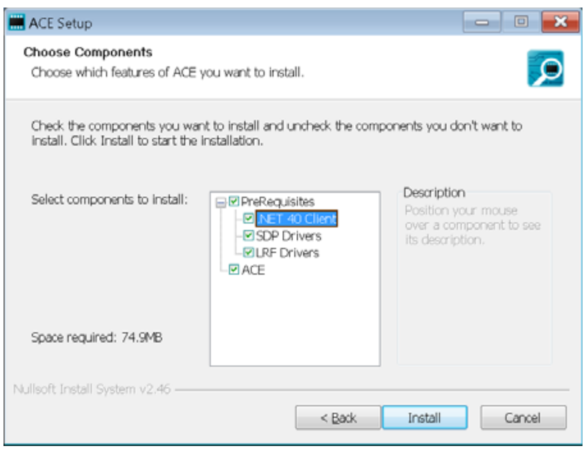
EVALUATION BOARD SOFTWARE QUICK START PROCEDURES

INSTALLING THE ACE SOFTWARE AND ADMV1014 PLUGINS AND DRIVERS

The ADMV1014-EVALZ software uses the Analog Devices, Inc., ACE software. Instructions on how to install and use the ACE software are available at www.analog.com/ACE.

If the ACE software has already been installed, ensure that the software is the latest version as shown on the www.analog.com/ACE page.
If the software is not the latest version, take the following steps:

1. Uninstall the current version of the ACE software.
2. Delete the **ACE** folder in **C:\ProgramData\Analog Devices**.
3. Install the latest version of the ACE software. During the installation, ensure that the SDP, LRF, and .Net driver installations are checked as well (see Figure 8).



17173-008

Figure 8. Required Drivers to Install with ACE

After the ACE software is installed, USB drivers must also be installed to use the ADMV1014-EVALZ evaluation board. These drivers are available for download and installation on the ADMV1014 product page.

After the ACE software is installed, download the **Board.ADMV1014.ace.zip** file from the ADMV1014 product page. After the download is finished, double-click the **Board.ADMV4420.ace.zip** file to complete the ADMV1014 plugin are installations on the ACE software.

Alternatively, in the main ACE window, click **Tools** > **Manage Plugins** > **Available Plugins**, and then search for **Board.ADMV1014** in the search bar. Highlight the search result and click **Install Selected** (see Figure 9).

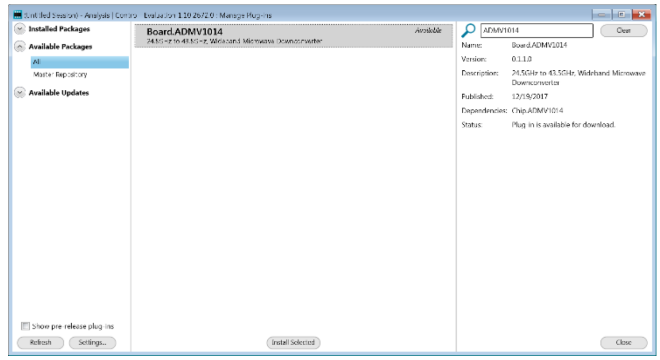
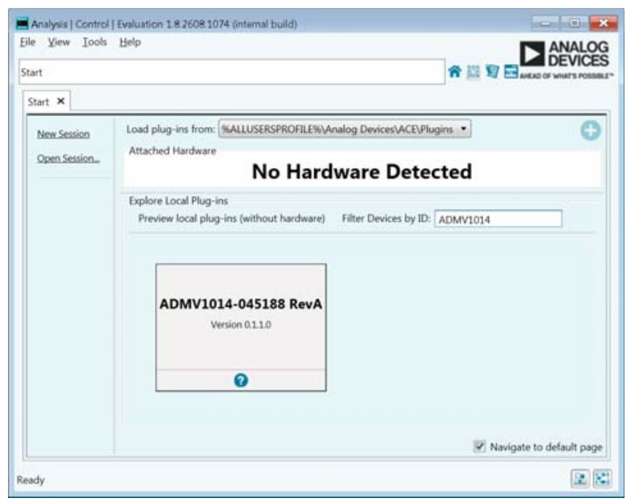


Figure 9 Installing the ADMV1014 Plugin from ACE

After the installations are complete, the ADMV1014-EVALZ evaluation board plugin appears when opening the ACE software (see Figure 10).



17173-009

Figure 10. ADMV1014-EVALZ Evaluation Board Plugin Window After Opening the ACE Software

INITIAL SETUP

To set up the ADMV1014-EVALZ evaluation board, take the following steps:

1. Connect a USB cable to the PC and then to the ADMV1014-EVALZ evaluation board.
2. Power up the ADMV1014-EVALZ evaluation board with a 5 V dc supply. When the USB cable is connected to the PC, the red LED lights up. The PC recognizes the ADMV1014-EVALZ evaluation board as the **ADMV1014-045188 RevA**.
3. Press the S1 button to hard reset the ADMV1014.
4. Open the ACE software. The **ADMV1014-045188 RevA** (ADMV1014-EVALZ) appears in the **Attached Hardware** section (see Figure 11). Double-click the evaluation board plugin.

Note that when the device is turned off and on while the ACE software is open, or when the USB cable is unplugged and plugged back in while the ACE software is open, contact with the ADMV1014-EVALZ evaluation board is lost. To regain contact, click the **System** tab, then click the **USB** symbol on the ADMV1014 subsystem, and then click **Acquire**. This command allows the user to reconnect to the ADMV1014-EVALZ evaluation board again. In some cases, this may not work and the user must close the ACE session by clicking the **File menu** and then clicking **Close Session**.

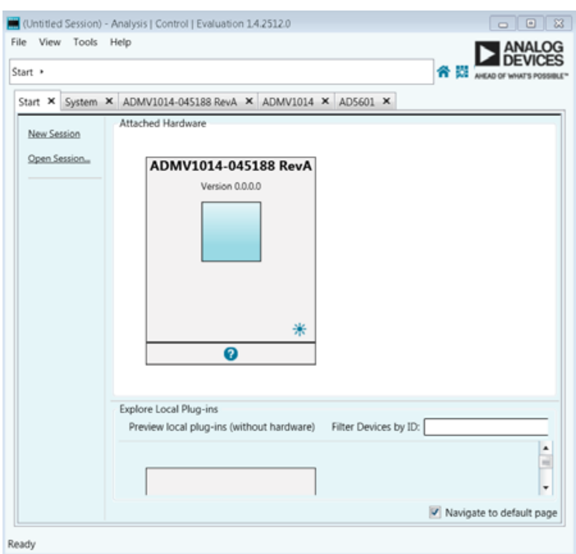


*Figure 11. Attached Hardware Section when the **ADMV1014-045188 RevA** (ADMV1014-EVALZ) is Connected*

5. The **ADMV1014-045188 RevA** tab opens. On the left side of the screen, click **Initial Configuration** to open this menu. Go to **Gain Setup** to enter the VCTRL voltage Note that 0 mV is the highest gain for the device (see Figure 12).
6. Click **Apply**, then click **Reset Board**, and then double-click **ADMV1014** (see the middle of the screen shown in Figure 12). For optimal performance, it is recommended to click **Reset Board** each time the USB is plugged in to the computer.

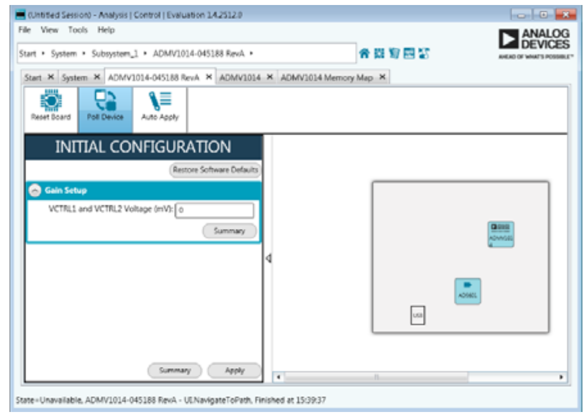


Figure 12. Initial Configuration for the Gain Setup and Board Plugin View

7. The ADMV1014 block diagram appears (see Figure 13).

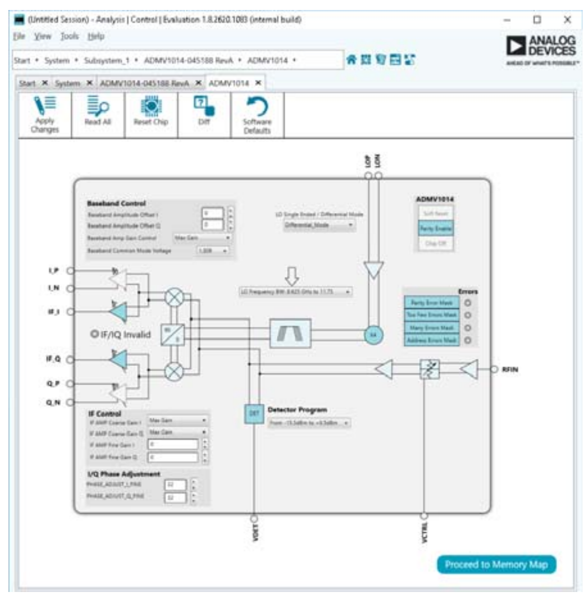


Figure 13. ADMV1014 Block Diagram in the ACE Software

ADMV1014 BLOCK DIAGRAM AND FUNCTIONS

The ADMV1014 ACE plugin is organized so that it appears similar to the block diagram shown in the ADMV1014 data sheet. This graphical user interface (GUI) layout correlates the functions on the ADMV1014-EVALZ evaluation board with the descriptions in the ADMV1014-EVALZ user guide. A full description of each block, register, and the corresponding settings is shown in the ADMV1014 data sheet. Some of the blocks and their functions are described as they pertain to the ADMV1014-EVALZ evaluation board. The full screen ADMV1014 block diagram, with labels, is shown in Figure 14. Table 1 describes the functionality of each block.

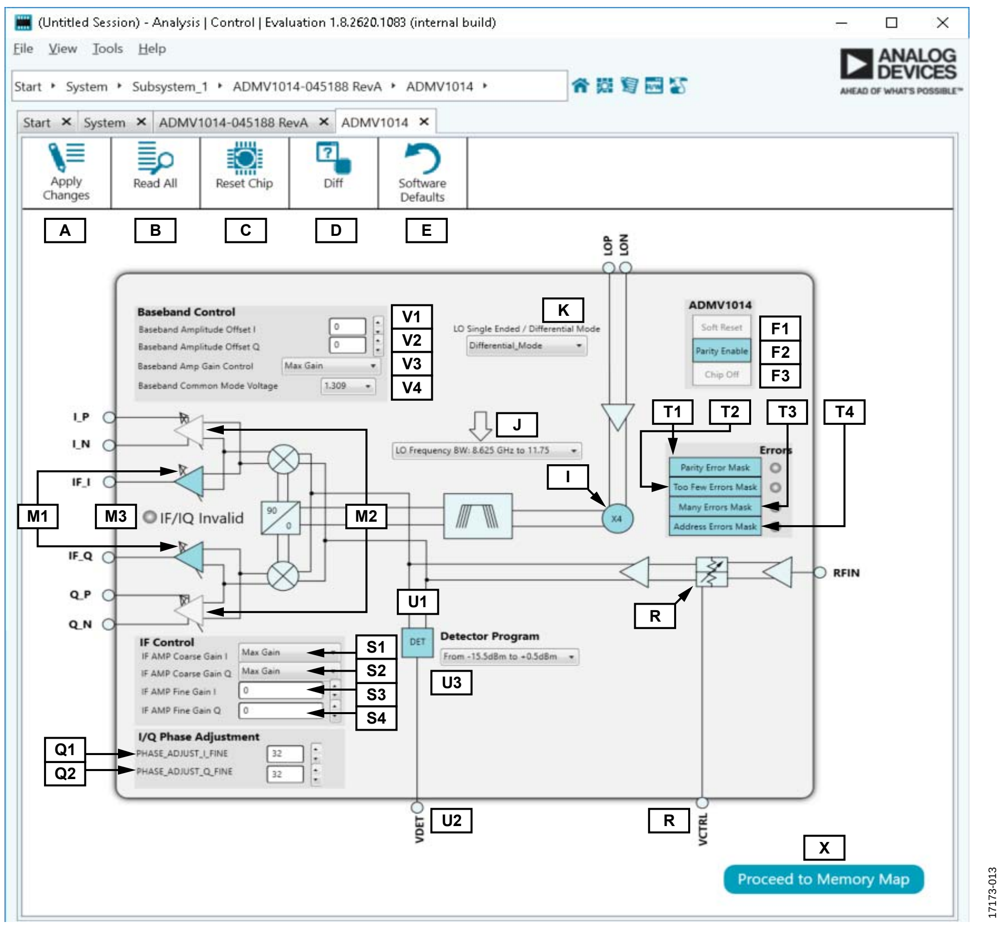


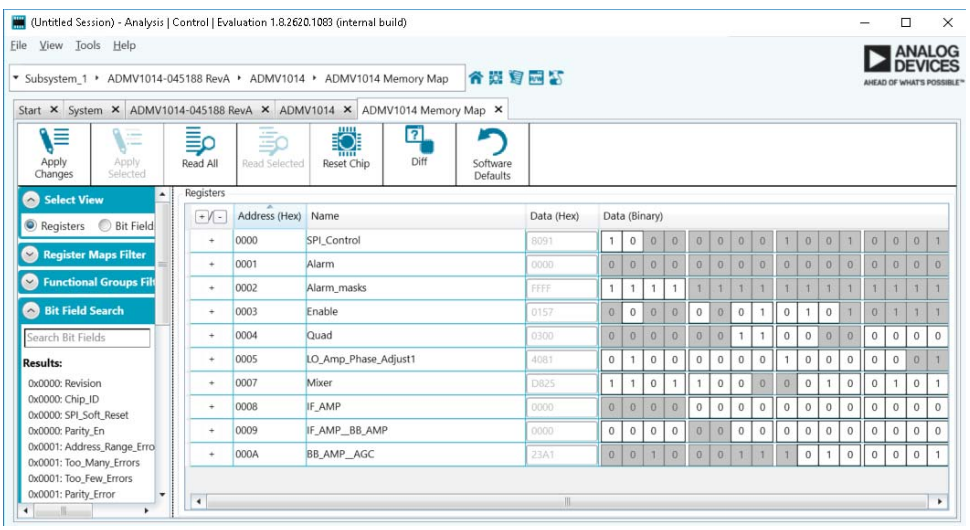
Figure 14. ADMV1014 Block Diagram with Labels

Table 1. ADMV1014 Block Diagram Label Functions (See Figure 14)

Label	Function
A	To apply all of the register values to the device, click **Apply Changes** (Label A). If **Auto Apply** is highlighted in the **ADMV1014-045188 RevA** tab, the **Apply Changes** feature (Label A) and the **Read All** feature (Label B) continuously run every few seconds, and **Apply Changes** (Label A) and **Read All** (Label B) do not need to be clicked to apply or read back the block diagram settings.
B	To read back all of the SPI registers of the device, click **Read All** (Label B). If **Auto Apply** is highlighted in the **ADMV1014-045188 RevA** tab, the **Apply Changes** feature (Label A) and the **Read All** feature (Label B) continuously run every few seconds, and **Apply Changes** (Label A) and **Read All** (Label B) do not need to be clicked to apply or read back the block diagram settings.
C	Click **Reset Chip** (Label C) to reset the 1.8 V SPI. **Reset Chip** has similar functionality as **Reset** (Label F1).
D	Click **Diff** (Label D) to show the registers that are different on the device.
E	Click **Software Defaults** (Label E) to load the software defaults on to the device, and then click **Apply Changes** (Label A).
F1	Click **Reset** (Label F1) to reset the ADMV1014 memory map.
F2	Click **Parity Enable** (Label F2) and then **Apply Changes** (Label A) to set the PARITY_EN bitfield (Bit 15, Register 0x00). When **Parity Enable** is highlighted, the PARITY_EN bitfield is enabled. When **Parity Enable** is not highlighted, the PARITY_EN bitfield is disabled.

Label	Function
F3	Click **Chip Off** (Label F3) and then **Apply Changes** (Label A) to set the IBIAS_PD bitfield (Bit 14, Register 0x03) and the BG_PD bitfield bit (Bit 5, Register 0x03). When **Chip Off** is highlighted, the chip is powered down. When **Chip Off** is not highlighted, the bit is disabled and the chip is powered up.
I	Click **Quadrupler On** (Label I) and **Apply Changes** (Label A) to set the QUAD_BG_PD bitfield (Bit 9, Register 0x03) and the QUAD_IBIAS_PD bitfield (Bit 7, Register 0x03). When **Quadrupler On** is highlighted, these two bits are disabled. When **Quadrupler On** is not highlighted, these two bits are enabled and the quadrupler is powered down.
J	Click the dropdown list on the band-pass filter to set the **LO Bandpass Filter** (Label J) and **Apply Changes** (Label A) to set the quad filters bitfield (Bits[3:0], Register 0x04) to choose the appropriate LO input bandwidth.
K	Choose the appropriate **LO differential/ single ended mode** (label K) and click **Apply Changes (**Label A) to set the QUAD_SE_MODE bitfield (Bits[9:6], Register 0x04). There are three options: differential, single-ended positive side, and single-ended negative side.
M1 to M3	IF and IQ path block. Click **IF Enable** (Label M1) and **Apply Changes** (Label A) to set the IF_AMP_PD bitfield (Bit 11, Register 0x03). When **IF Enable** is highlighted, the IF_AMP_PD bitfield is disabled. When **IF Enable** is not highlighted, the bit is enabled and the mixer is powered down. Click **BB Enable** (Label M2) and **Apply Changes** (Label A) to set the BB_AMP_PD bitfield (Bit 8, Register 0x03). When **BB Enable** is highlighted, the bitfield is disabled. When **BB Enable** is not highlighted, the bitfield is enabled and the mixer is powered down. If **BB Enable** and **IF Enable** are both highlighted, then **IF/IQ Invalid Path Invalid** (Label M3) and the red LED turns on to indicate this mode of operation is not recommended.
Q1 to Q2	I/Q phase adjustment blocks (**Phase Adjust I_FINE** and **Phase Adjust Q_FINE**). Click the spin box or enter a value between 0 and 127 in the **Phase Adjust I_FINE** box (Label Q1) and click **Apply Changes** (Label A) to set the LOAMP_PH_ADJ_I_FINE bitfield (Bits[15:9], Register 0x06). Click the spin box or enter a value between 0 and 127 in the **Phase Adjust Q_FINE** box (Label Q2) and click **Apply Changes** (Label A) to set the LOAMP_PH_ADJ_Q_FINE bitfield (Bits[8:2], Register 0x06).
R	See the Setting VCTRL Voltage for the ADMV1014 section for additional details.
S1 to S4	IF control. Click the dropdown list for **IF AMP Coarse Gain I** box (Label S1) and **Apply Changes** (Label A) to set the IF_AMP_FINE_GAIN_I bitfield (Bits[11:8], Register 0x08). There are five options: maximum, minimum, and attenuation by 0.8 dB, 1.6 dB, and 2.4 dB. Click the dropdown list for **IF AMP Coarse Gain Q** box (Label S2) and **Apply Changes** (Label A) to set the IF_AMP_FINE_GAIN_Q bitfield (Bits[15:12], Register 0x09). There are five options: maximum, minimum, and attenuation by 0.8 dB, 1.6 dB, and 2.4 dB. Click the spin box or enter a value between 0 and 15 in **IF AMP Fine Gain I** box (Label S3) and **Apply Changes** (Label A) to set the IF_AMP_FINE_GAIN_I bitfield (Bits[3:0], Register 0x08). Click the spin box or enter a value between 0 and 15 in **IF AMP Fine Gain Q** box (Label S4) and **Apply Changes** (Label A) to set the IF_AMP_FINE_GAIN_Q bitfield (Bits[7:4], Register 0x08).
T1 to T4	Error mask and readback operations are as follows: Click **Parity Error Mask** (Label T1) and **Apply Changes** (Label A) to set the PARITY_ERROR_MASK bitfield (Bit 15, Register 0x02). When **Parity Errors Mask** is highlighted, the PARITY_ERROR_MASK bitfield is enabled. When **Parity Error Mask** is not highlighted, the PARITY_ERROR_MASK bitfield is disabled. Click **Too Few Errors Mask** (Label T2) and **Apply Changes** (Label A) to set the TOO_FEW_ERRORS_MASK bitfield (Bit 14, Register 0x02). When **Too Few Errors Mask** is highlighted, the TOO_FEW_ERRORS_MASK bitfield is enabled. When **Too Few Errors Mask** is not highlighted, the TOO_FEW_ERRORS_MASK bitfield is disabled. Click **Many Errors Mask** (Label T3) and **Apply Changes** (Label A) to set the TOO_MANY_ERRORS_MASK bitfield (Bit 13, Register 0x02). When **Many Errors Mask** is highlighted, the TOO_MANY_ERRORS_MASK bitfield is enabled. When **Many Errors Mask** is not highlighted, the TOO_MANY_ERRORS_MASK bitfield is disabled. Click **Address Errors Mask** (Label T4) and **Apply Changes** (Label A) to set the ADDRESS_RANGE_ERROR_MASK bitfield (Bit 12, Register 0x02). When **Address Errors Mask** is highlighted, the ADDRESS_RANGE_ERROR_MASK bitfield is enabled. When **Address Errors Mask** is not highlighted, the ADDRESS_RANGE_ERROR_MASK bitfield is disabled. When the PARITY_ERROR_MASK bitfield (Bit 15, Register 0x02) is set, **Parity Error Mask** lights up green when then the PARITY_ERROR bitfield (Bit 15, Register 0x01) is toggled. When the TOO_FEW_ERRORS_MASK bitfield (Bit 14, Register 0x02) is set, **Too Few Errors Mask** lights up green when the TOO_FEW_ERRORS bitfield (Bit 14, Register 0x01) is toggled. When the TOO_MANY_ERRORS_MASK bitfield (Bit 13, Register 0x02) is set, **Too Many Errors Mask** lights up green when the TOO_MANY_ERRORS bitfield (Bit 13, Register 0x01) is toggled. When the ADDRESS_RANGE_ERROR_MASK bitfield (Bit 12, Register 0x02) is set, **Address Errors Mask** lights up green when the ADDRESS_RANGE_ERROR bitfield (Bit 12, Register 0x01) is toggled.

Label	Function
U1 to U3	Detector. Click **Detector Enable** (Label U1) and **Apply Changes** (Label A) to set the DET_EN bitfield (Bit 6, Register 0x03). This action turns on the detector. When **Detector Enable** is highlighted, the DET_EN bitfield is enabled. When **Detector Enable** is highlighted, the DET_EN bitfield is disabled. The output of the envelope detector is on **VDET** (Label U2) connector. Click the dropdown list for the **Detector Program** (Label U3) box to set DET_PROG bitfield (Bits[6:0], Register 0x07). There are eight options.
V1 to V4	Baseband control. Click the spin box or enter a value between −15 and +15 in the **Baseband Amplitude Offset I** box (Label V1), and then click **Apply Changes** (Label A) to set the BB_AMP_OFFSET_I bitfield (Bits[4:0], Register 0x09). Click the spin box or enter a value between −15 and +15 in the **Baseband Amplitude Offset Q** box (Label V2), and then click **Apply Changes** (Label A) to set the BB_AMP_OFFSET_Q bitfield (Bits[9:5], Register 0x09). Click the spin box or enter a value between 0 and 3 for **Baseband Amp Gain Control** box (Label V3), and then click **Apply Changes** (Label A) to set BB_AMP_GAIN_CTRL bitfield (Bits[2:1], Register 0xA). Use the **Baseband Common Mode Voltage** box (Label V4) and click **Apply Changes** (Label A) to set the baseband common-mode voltage. This action sets the BB_LOW_COMMON_MODE_EN bitfield (Bits[0], Register 0xA), MIXER_VGATE bitfield (Bits[15:9]. Register 0x7), and BB_AMP_REF_GEN bitfield (Bits[6:3], Register 0xA). Refer to the ADMV1014 data sheet for more information.
X	Click **Proceed to Memory Map** (Label X) to open the ADMV1014 memory map (see Figure 15).



17173-014

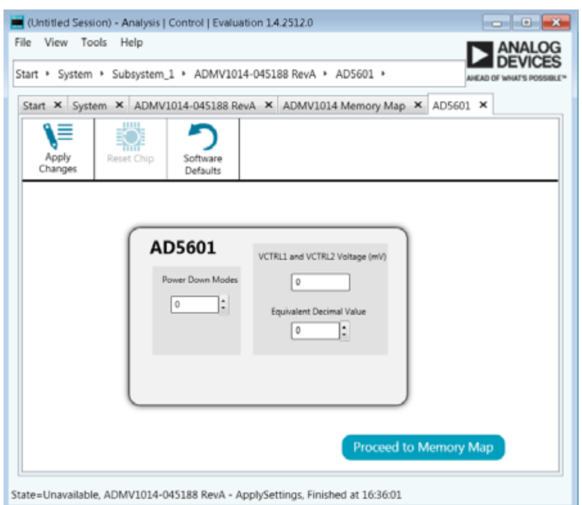
Figure 15. ADMV1014 Memory Map in the ACE Software

SETTING VCTRL VOLTAGE FOR THE ADMV1014

The ADMV1014-EVALZ evaluation board comes with the AD5601 *nano*DAC. The AD5601 *nano*DAC sets the control voltage for the VCTRL pin of the ADMV1014. When the ADMV1014-EVALZ evaluation board plugin is open, set the voltage in the **Initial Configuration** menu. Note that 0 mV is the highest gain setting for the devices.

When using an external power supply for the VCTRL voltage, use the AD5601 *nano*DAC plugin to change the voltage or to power down the *nano*DAC. To open the *nano*DAC plugin, click the AD5601 tab at the top of the ACE software window or double-click **AD5601** within the **ADMV1014-045188, Rev. A** tab (see Figure 12). Figure 16 shows the AD5601 *nano*DAC user interface. The user interface contains the **Power Down Modes** section and the VCTRL voltage section.

To power up or power down the AD5601 *nano*DAC, go to the **Power Down Modes** section. To use the AD5601 *nano*DAC, set the **Power Down Modes** box to 0. When the VCTRL voltage is being applied externally, set the **Power Down Modes** box to 1, 2, or 3 through the test loop. For more information on the different power-down modes of the AD5601 *nano*DAC, see the power-down modes section of the AD5601 data sheet.



17173-015

Figure 16. AD5601 nano*DAC User Interface*

To set the VCTRL voltage, type a number in the **VCTRL and VCTRL2 Voltage (mV)** box or type the corresponding decimal number for an 8-bit register in the **Equivalent Decimal Value** box. The VCTRL range available is from 0 mV to 3300 mV. To set the lowest gain for the ADMV1014, set **VCTRL and VCTRL2 Voltage (mV)** to 1800. To set the highest gain for the ADMV1014, set **VCTRL and VCTRL2 Voltage (mV)** to 0. Note that, there is no change in the gain of the ADMV1014 above 1800 mV.

After making any changes to the voltage or the power-down mode, click **Apply Changes** shown in the top left of the ACE software window (see Figure 16). When **Auto Apply** is selected in the **ADMV1014-045188, Rev. A** tab, these changes take place automatically and there is no need to click **Apply Changes**.

UPDATING REGISTER 0x0B SEQUENCE

When Register 0x0B must be updated, the update must follow a specific sequence. The ACE software automatically follows this sequence when Register 0x0B is in need of an update. This update sequence for the ACE software is as follows:

1. Disable the PARITY_EN bit (Bit 15, Register 0x00).
2. Write to Register 0x0B.
3. Enable the PARITY_EN bit (Bit 15, Register 0x00).

TEST RESULTS

When testing the ADMV1014-EVALZ evaluation board, the results described in this section are the expected results. VCTRL = 0 mV is used for both the IF results and the I/Q results.

IF RESULTS

This section describes the expected results for IF mode. The hybrids, connectors, and evaluation board are not deembedded.

Figure 17 shows the results of an RF input of 29 GHz at −25 dBm, with a 7 GHz LO at 0 dBm to an IF output of 1 GHz for upper sideband settings.

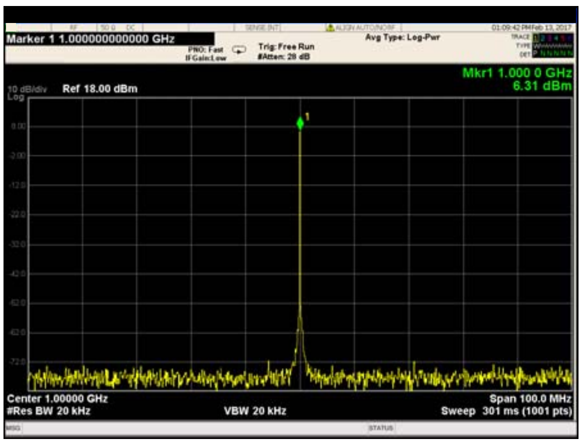


Figure 17. ADMV1014 Results for IF Mode

Figure 18 shows the GUI settings for the results shown in Figure 17.

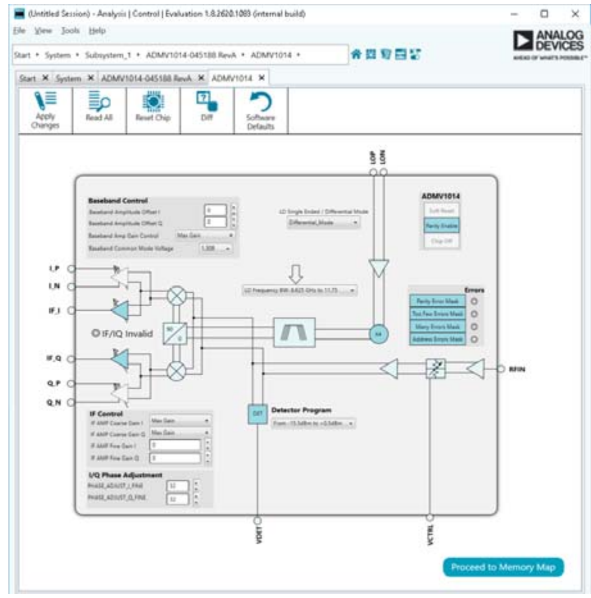


Figure 18. ADMV1014 GUI Settings for IF Mode

EVALUATION BOARD SCHEMATICS AND ARTWORK

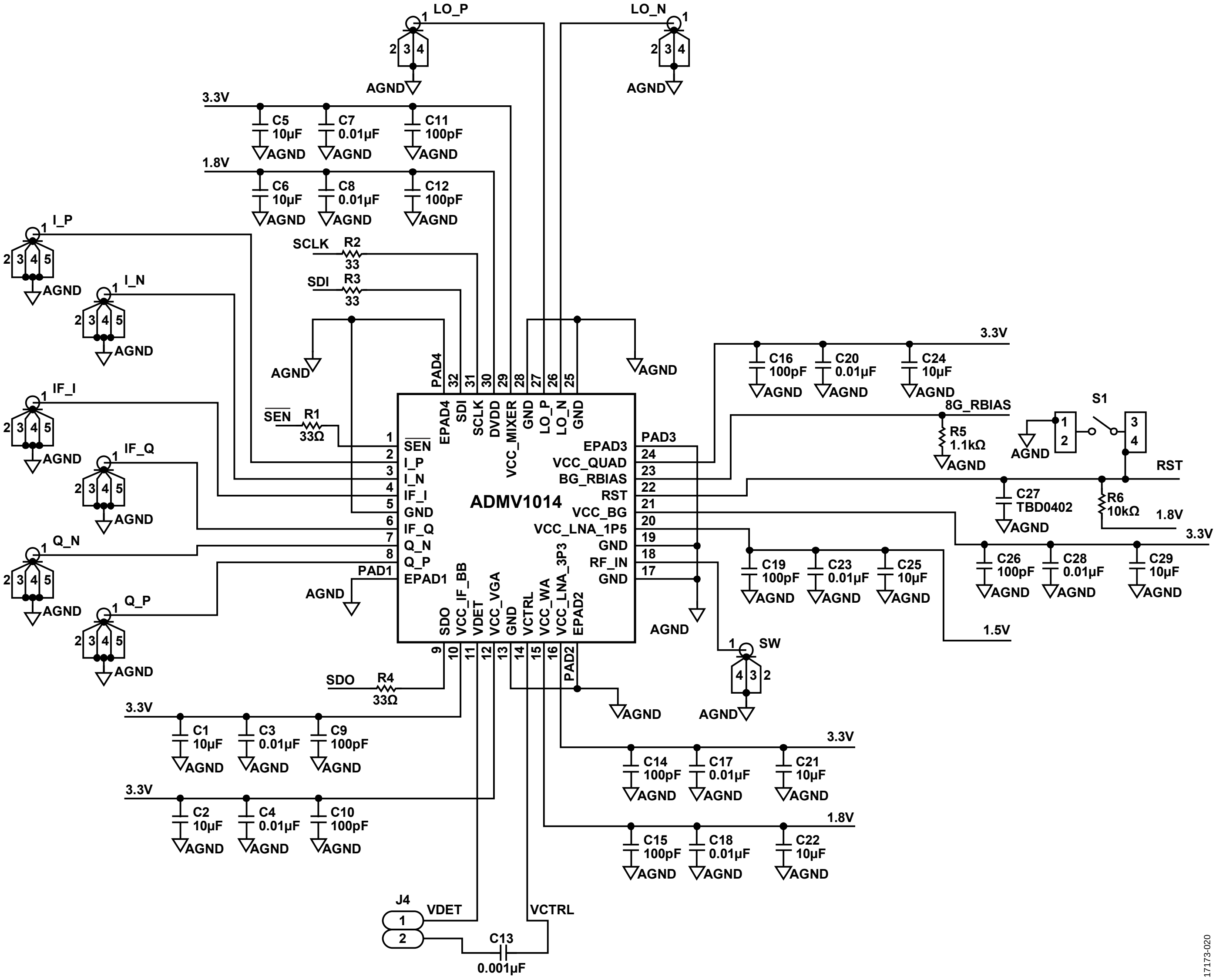


Figure 19. ADMV1014-EVALZ Evaluation Board Schematic—ADMV1014 Connections

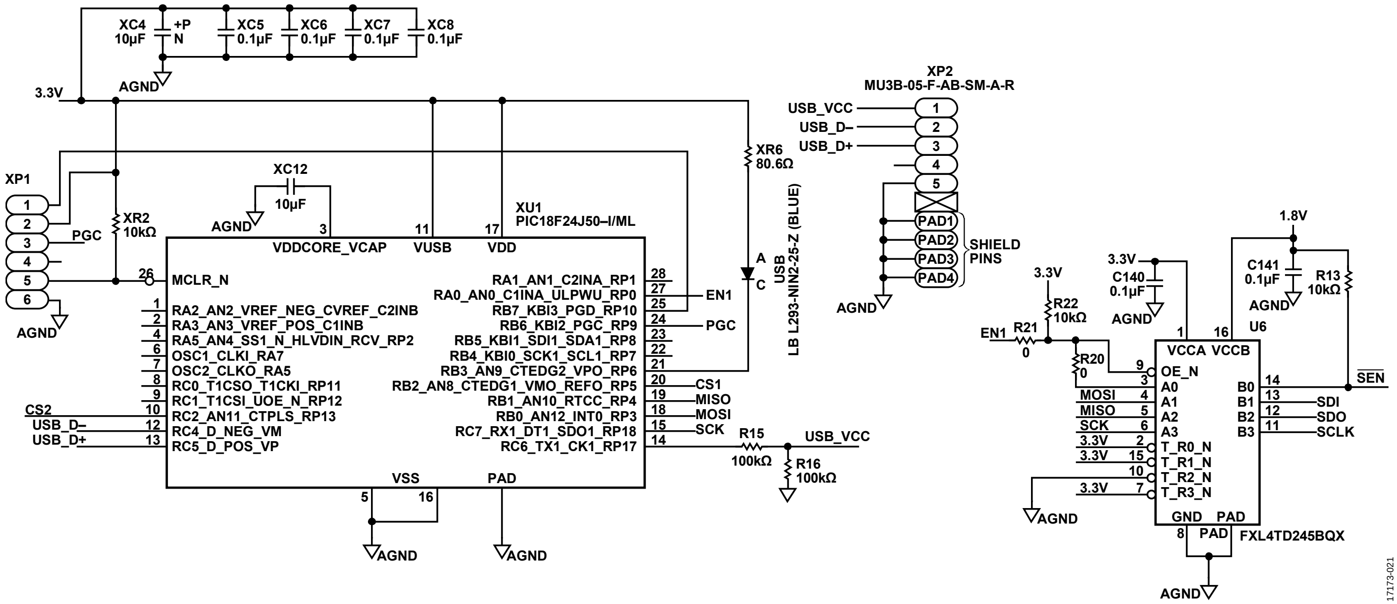


Figure 20. ADMV1014-EVALZ Evaluation Board Schematic—Microcontroller and Level Shifter Connections

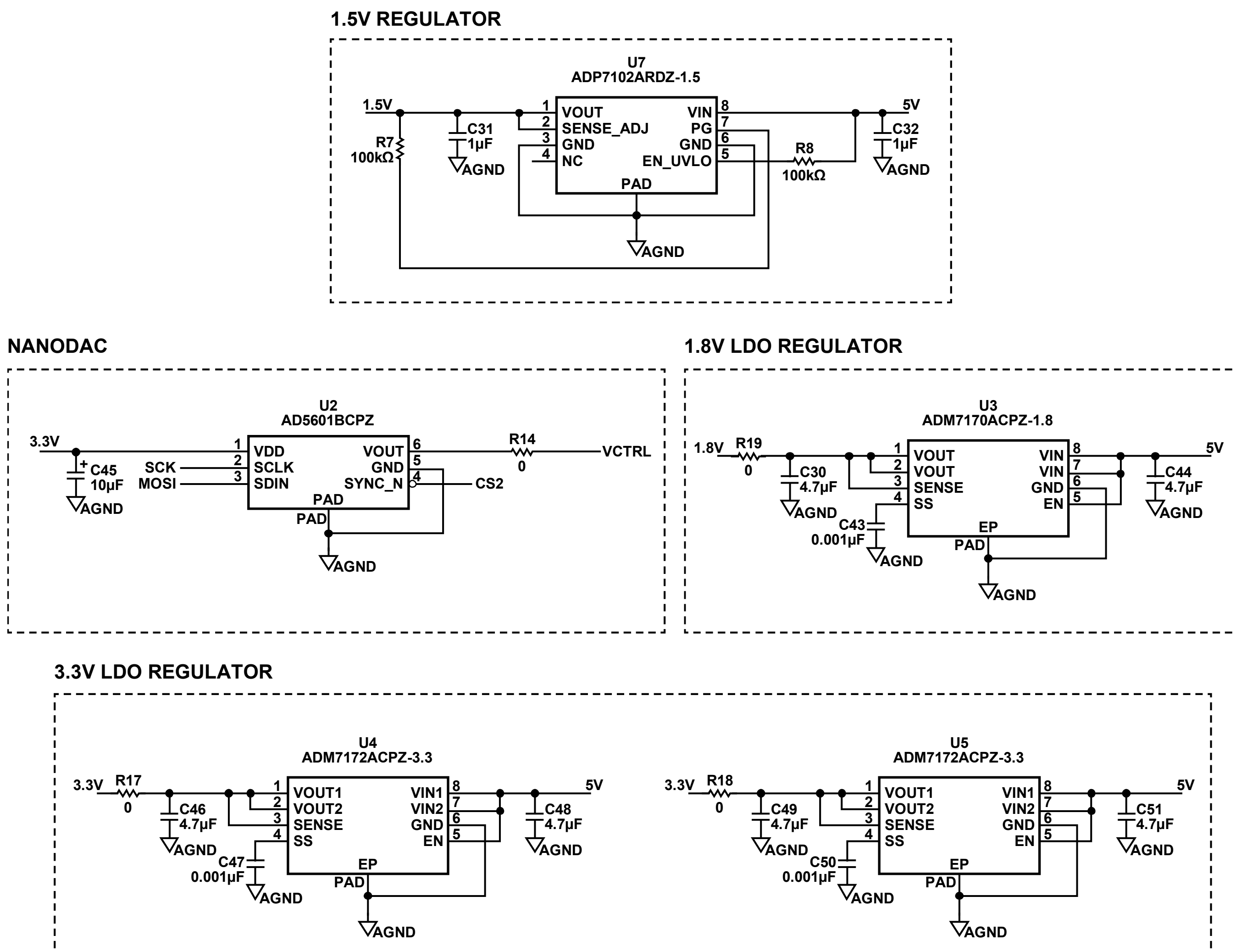


Figure 21. ADMV1014-EVALZ Evaluation Board Schematic—LDO Regulator Connections

ADMV1014-EVALZ EVALUATION BOARD ARTWORK

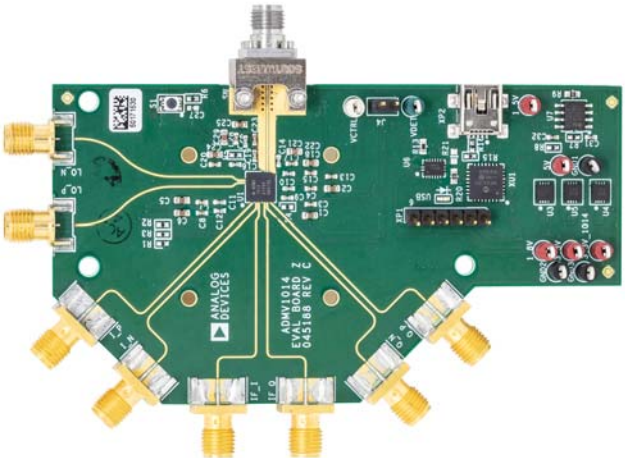


Figure 22. ADMV1014-EVALZ Evaluation Board, Top

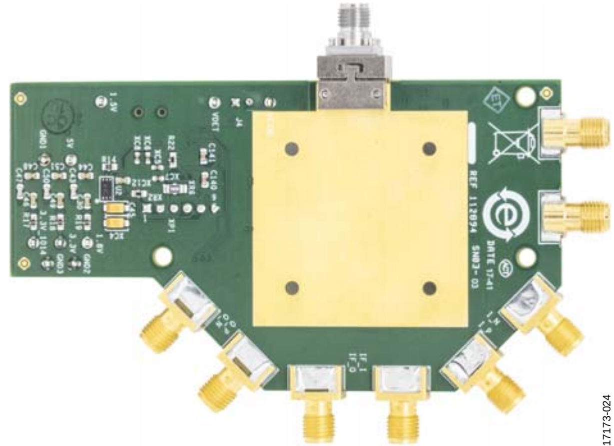
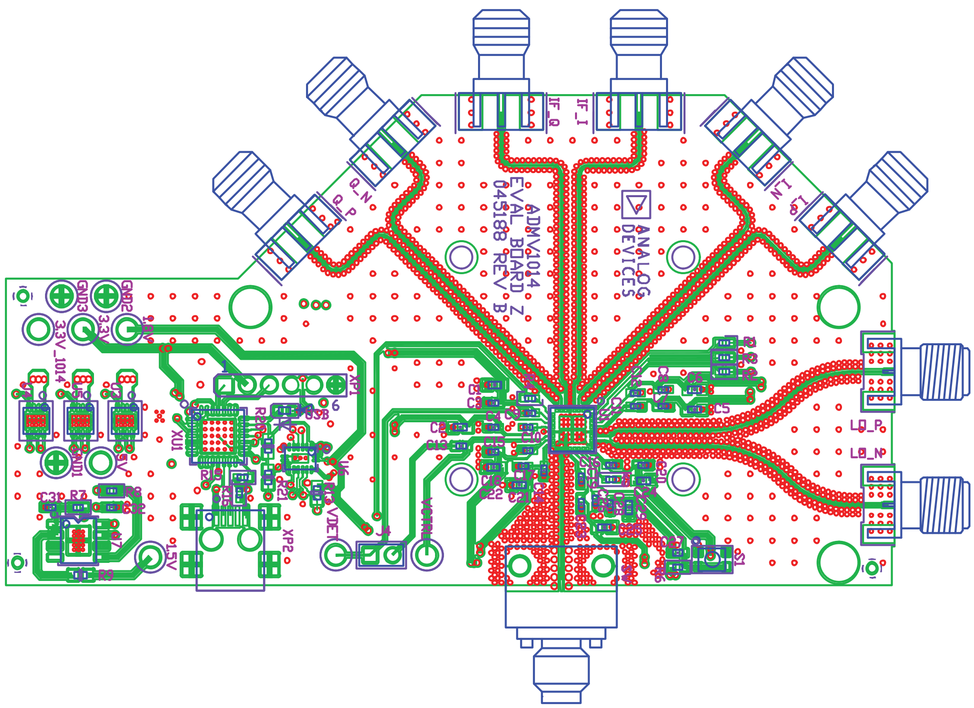


Figure 23. ADMV1014-EVALZ Evaluation Board, Bottom



NOTE
1. THE SILKSCREEN MIGHT BE SLIGHTLY DIFFERENT DEPENDING ON THE REVISION OF THE BOARD.

Figure 24. ADMV1014-EVALZ Evaluation Board Printed Circuit Board (PCB), Top Layer

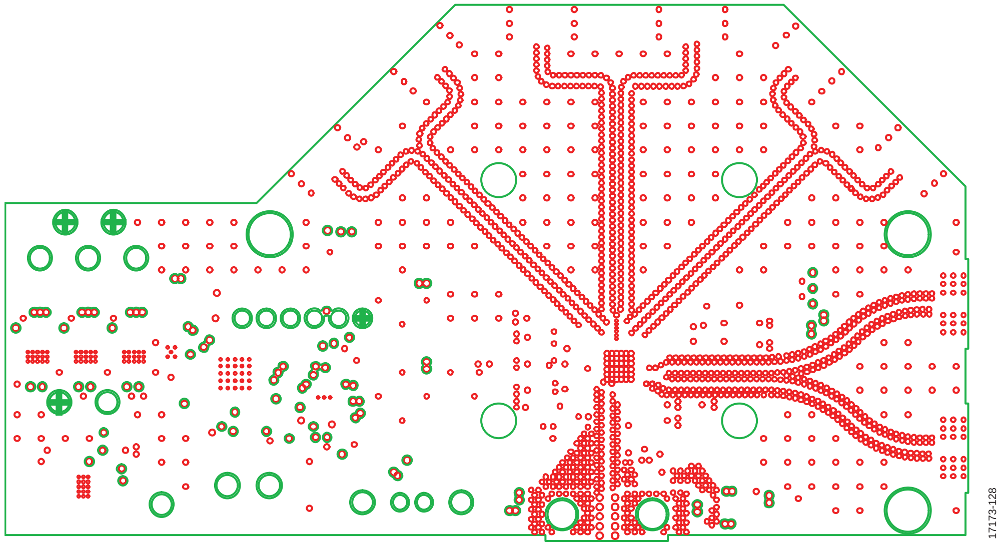


Figure 25. ADMV1014-EVALZ Evaluation Board PCB, Second Layer Voltages

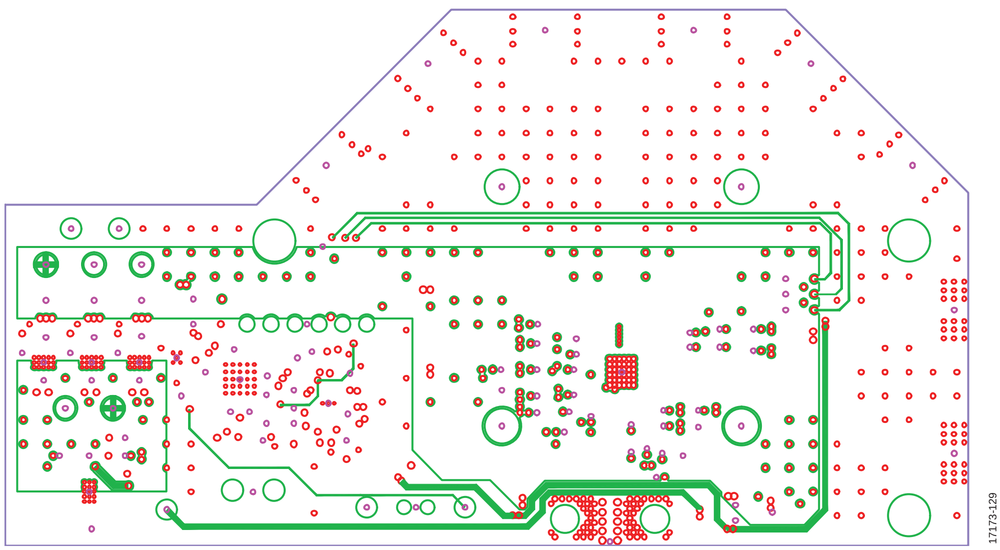


Figure 26. ADMV1014-EVALZ Evaluation Board PCB, Third Layer

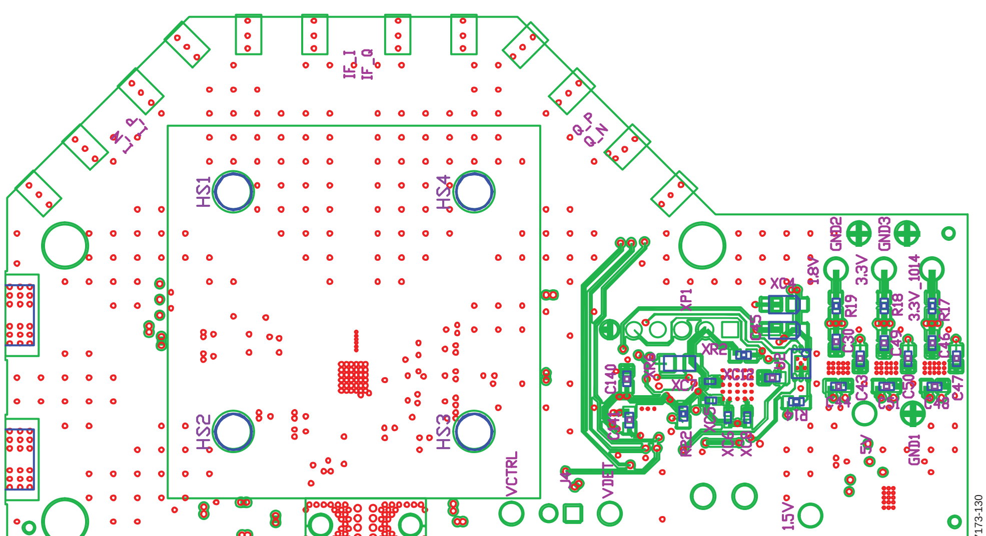


Figure 27. ADMV1014-EVALZ Evaluation Board PCB, Bottom Layer

CONFIGURATION OPTIONS

Table 2. ADMV1014-EVALZ Configuration Options (Bill of Materials)

Component	Function	Default Condition
1.5 V, 1.8 V, 3.3_1014, 3.3 V, 5 V, GND	Power supplies and ground	Not applicable
LON, LOP, IF_I, IF_Q, Q_P, Q_N, I_N, I_P, RFIN, VDET, VCTRL	Data and clock	Not applicable
SCLK, SDI, $\overline{\text{SEN}}$, SDO	SPI	Not applicable
R1 to R4	33 Ω series resistors for SPI pins	R1 to R4 = 33 Ω (0402)
R5	1.1 kΩ series resistors for BG pins	R5 = 1.1 kΩ (0402)
5 V, 3.3 V, 3.3V_1014, 1.8 V, 1.5 V, VCTRL, VDET, GND1 to GND3	Test points	Not applicable
R7, R8 , R14, R15, R16, R9, R17 to R20, XR6	Shorts or power supply decoupling resistors	R9, R14, R17 to R20 = 0 Ω (0603), R6, R15, R16 = 100 kΩ (0402), R7, R8 , R15, R16 = 100 kΩ (0603), XR6 = 80.6 Ω (1206)
R6, R13, R22, XR2	Pull-up or pull-down resistors	XR2, R13, R22 = 10 kΩ (0603), R6 = 10 kΩ (0402)
C2 to C4, C5, C11 to C31, C34 to C42, C43 to C51, XC12, XC4 to XC8, C5 to C26, C28 to 32, C43 to C51, C140, C141	The capacitors provide the required decoupling of the supply related pins	XC4, XC12, C1, C2, C5, C6, C21, C22, C24, C25, C29, C45 = 10 μF (0603), C31, C32 = 1 μF (0402), C30, C44, C46, C48, C49, C51 = 4.7 μF (0603), XC5, XC6, XC7, XC8 = 0.1 μF (0402), C13 = 1pF (0402), C43, C47, C50 = 1 pF (0603), C3, C4, C7, C8, C17, C18, C20, C23, C28 = 10 pF (0402), C9 to C12, C14 to C16, C19, C26, C140 to C141, XC5 to XC8 = 0.1 μF (0603)
R21, C27	Do not install (DNI)	R21, C27 = 0402
XP1	Programming header	Not applicable
XP2	Mini USB connector	Connect the mini USB cable to XP2 to interface with the SPI
S1	Reset button	Click RSTB to reset the device
USB	Red LED	LED is blue when the USB is connected to XP2, and the PC and the ADMV1014-EVALZ evaluation board is powered on with a 5 V supply
XU1	Microcontroller	PIC18F24J50
U6	Level shifter	FXL4TD245BQX
U3 to U5, U7	3.3 V and 1.8 V regulators	ADM7170 (U3) = 1.8 V regulator, ADM7172 (U4) = 3.3 V regulator, ADM7172 (U5) = 3.3 V regulator for the ADMV1014, ADM7172 (U7) = 1.5 V regulator,
U2	AD5601 *nano*DAC	Not applicable
DUT	ADMV1014 device under test	Not applicable
PCB	PCB, ADMV1014-EVALZ [1]	Not applicable

[1] The evaluation board material between Layer 1 and Layer 2 is made of 10.7 mil Rogers 4350B LOPRO®.

NOTES

ESD Caution

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Legal Terms and Conditions

By using the evaluation board discussed herein (together with any tools, components documentation or support materials, the "Evaluation Board"), you are agreeing to be bound by the terms and conditions set forth below ("Agreement") unless you have purchased the Evaluation Board, in which case the Analog Devices Standard Terms and Conditions of Sale shall govern. Do not use the Evaluation Board until you have read and agreed to the Agreement. Your use of the Evaluation Board shall signify your acceptance of the Agreement. This Agreement is made by and between you ("Customer") and Analog Devices, Inc. ("ADI"), with its principal place of business at One Technology Way, Norwood, MA 02062, USA. Subject to the terms and conditions of the Agreement, ADI hereby grants to Customer a free, limited, personal, temporary, non-exclusive, non-sublicensable, non-transferable license to use the Evaluation Board FOR EVALUATION PURPOSES ONLY. Customer understands and agrees that the Evaluation Board is provided for the sole and exclusive purpose referenced above, and agrees not to use the Evaluation Board for any other purpose. Furthermore, the license granted is expressly made subject to the following additional limitations: Customer shall not (i) rent, lease, display, sell, transfer, assign, sublicense, or distribute the Evaluation Board; and (ii) permit any Third Party to access the Evaluation Board. As used herein, the term "Third Party" includes any entity other than ADI, Customer, their employees, affiliates and in-house consultants. The Evaluation Board is NOT sold to Customer; all rights not expressly granted herein, including ownership of the Evaluation Board, are reserved by ADI. CONFIDENTIALITY. This Agreement and the Evaluation Board shall all be considered the confidential and proprietary information of ADI. Customer may not disclose or transfer any portion of the Evaluation Board to any other party for any reason. Upon discontinuation of use of the Evaluation Board or termination of this Agreement, Customer agrees to promptly return the Evaluation Board to ADI. ADDITIONAL RESTRICTIONS. Customer may not disassemble, decompile or reverse engineer chips on the Evaluation Board. Customer shall inform ADI of any occurred damages or any modifications or alterations it makes to the Evaluation Board, including but not limited to soldering or any other activity that affects the material content of the Evaluation Board. Modifications to the Evaluation Board must comply with applicable law, including but not limited to the RoHS Directive. TERMINATION. ADI may terminate this Agreement at any time upon giving written notice to Customer. Customer agrees to return to ADI the Evaluation Board at that time. LIMITATION OF LIABILITY. THE EVALUATION BOARD PROVIDED HEREUNDER IS PROVIDED "AS IS" AND ADI MAKES NO WARRANTIES OR REPRESENTATIONS OF ANY KIND WITH RESPECT TO IT. ADI SPECIFICALLY DISCLAIMS ANY REPRESENTATIONS, ENDORSEMENTS, GUARANTEES, OR WARRANTIES, EXPRESS OR IMPLIED, RELATED TO THE EVALUATION BOARD INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTY OF MERCHANTABILITY, TITLE, FITNESS FOR A PARTICULAR PURPOSE OR NONINFRINGEMENT OF INTELLECTUAL PROPERTY RIGHTS. IN NO EVENT WILL ADI AND ITS LICENSORS BE LIABLE FOR ANY INCIDENTAL, SPECIAL, INDIRECT, OR CONSEQUENTIAL DAMAGES RESULTING FROM CUSTOMER'S POSSESSION OR USE OF THE EVALUATION BOARD, INCLUDING BUT NOT LIMITED TO LOST PROFITS, DELAY COSTS, LABOR COSTS OR LOSS OF GOODWILL. ADI'S TOTAL LIABILITY FROM ANY AND ALL CAUSES SHALL BE LIMITED TO THE AMOUNT OF ONE HUNDRED US DOLLARS ($100.00). EXPORT. Customer agrees that it will not directly or indirectly export the Evaluation Board to another country, and that it will comply with all applicable United States federal laws and regulations relating to exports. GOVERNING LAW. This Agreement shall be governed by and construed in accordance with the substantive laws of the Commonwealth of Massachusetts (excluding conflict of law rules). Any legal action regarding this Agreement will be heard in the state or federal courts having jurisdiction in Suffolk County, Massachusetts, and Customer hereby submits to the personal jurisdiction and venue of such courts. The United Nations Convention on Contracts for the International Sale of Goods shall not apply to this Agreement and is expressly disclaimed.

UG17173-0-4/19(A)