

Keywords: filter, filter network, switched-capacitor filter, anti-aliasing, sinc compensation, spectral energy, DAC quantization noise

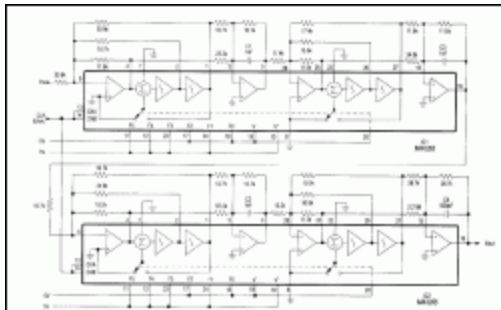
## APPLICATION NOTE 29

# Multipurpose Filter Network Combines Anti-Aliasing and Sinc Compensation

Jul 09, 1998

*Abstract: In this application note a circuit with two switched-capacitor filters reconstructs the output of a digital-to-analog converter (DAC) while providing anti-aliasing and sinc-compensation functions. Filter IC prevents alias frequencies by excluding spectral energy above  $f_s/2$ . The MAX265 filter is featured.*

The dual-biquad filter chips and some external components (**Figure 1**) form a multipurpose filter for the reconstruction of D/A converter signals. Connected to a converter's output (**Figure 2**), the filter aids in generating the analog signal represented by digital-data samples at the converter's input. In addition, the filter provides anti-aliasing,  $(\sin\pi x)/\pi x$  (sinc) compensation, and reduction of the D/A converter's quantization noise.



[More detailed image](#)

Figure 1. Configured as shown, two filter ICs reconstruct the output of D/A converter while providing antialiasing and sinc-compensation functions.

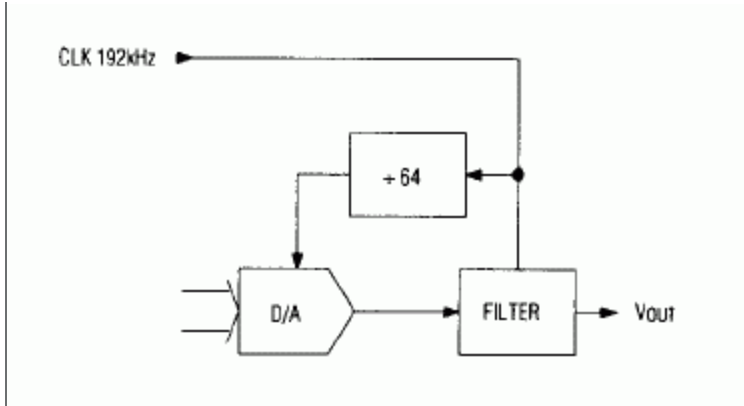


Figure 2. In a suggested application for the Figure 1 circuit, the applied clock signal and single-chip divider set the desired sample rate for the D/A converter.

At DC, a D/A converter's output is easily predicted from its data sheet specs. Time-varying signals, however, produce staircase-output waveforms whose reconstruction errors are best discussed in the frequency domain. The converter's output spectrum, for example, consists of spectra ( $\pm f_1$ , where  $f_1$  is the spectrum represented by the digital input samples) that repeat at integral multiples of the sample rate  $f_S$  (Figure 3).

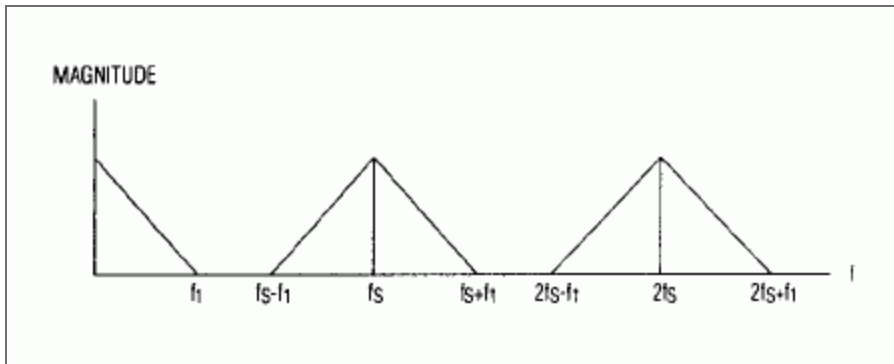


Figure 3. Figure 2's digital-input spectrum  $F_1$  combines with the D/A converter's sampling rate  $f_S$  as shown, producing a  $\pm f_1$  spectrum that repeats at integral multiples of  $f_S$ .

The filter's first job is to prevent alias frequencies by excluding spectral energy above  $f_S/2$ . In practice,  $f_1 < f_S/2$ . The filter should pass  $f_1$  with an acceptably low error while sufficiently attenuating all frequencies above  $f_S/2$ .

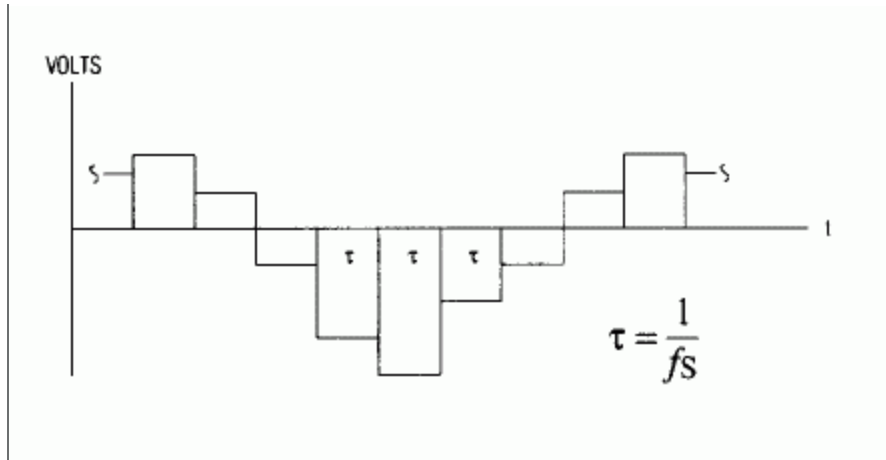


Figure 4. Before filtering, the D/A converter's output signal is a staircase waveform that can be regarded as a sequence of rectangular pulses.

A second filter requirement stems from the presence of sinc attenuation, introduced by the effect of rectangular-pulse components in the staircase waveform (**Figure 4**). These pulses have the same  $1/f_S$  width, but differ in amplitude according to the digital-sample magnitudes. The spectrum of each pulse is the Fourier transform (the sinc function of  $f/f_S$ ). These spectra combine with the  $f_1$  spectrum to form an overall frequency response for the converter output. Note the sinc expression's variation in amplitude for various values of  $f$ :

Table 1.

$f$	$[(\sin)(\pi f/f_S)]/(\pi f/f_S)$
0	1.0
$f_S/4$	0.9003 (-0.9dB)
$f_S/3$	0.8270 (-1.65dB)
$f_S/2$	0.6366 (-3.92dB)

Clearly, the staircase approximation causes an increase amplitude error as  $f$  approaches the Nyquist frequency  $f_S/2$ . To compensate for this attenuation, the Figure 1 circuit incorporates the inverse expression  $(\pi f/f_S)/\sin(\pi f/f_S)$  in its passband-magnitude response.

Ideally, the resulting filter response would provide sinc compensation to  $f_S/2$ , drop abruptly to zero, and maintain that infinite attenuation for all frequencies above  $f_S/2$ . But actual filters cannot provide abrupt transitions or infinite attenuation. As a practical compromise, the circuit makes its transition over a finite bandwidth (transition ratio), and then provides an out-of-band rejection comparable to the D/A converter's signal-to-noise ratio SNR.

SNR for an ideal D/A converter is about 6dB/bit, or 72dB for a 12-bit device. Quantization error further degrades this number, yielding about 68dB for a typical 12-bit converter. Thus a reasonable goal in Figure 1 is 70dB rejection above  $f_S/2$ .

To prevent aliasing, the stopband edge must be no greater than the Nyquist frequency ( $f_S/2$ ). The passband edge must therefore be less than  $f_S/2$ . To achieve 70dB stopband rejection in the 8th-order

circuit of Figure 1, the required transition ratio ( $f_{\text{Stopband}}/f_{\text{Passband}}$ ) is 1.5, which sets the passband edge at  $f_S/3$ . A rising amplitude response within this passband compensates for the converter's sinc attenuation.

Perfect sinc compensation would provide 1.65dB of gain at the Nyquist frequency, but tolerance uncertainties in the  $\pm 1\%$  resistors and within the filter ICs limits the actual correction to about 1dB. The circuit does, however, achieve the 70dB stopband rejection and the 1.5 transition ratio. **Figure 5** compares the Figure 1 response with that of an ideal filter.

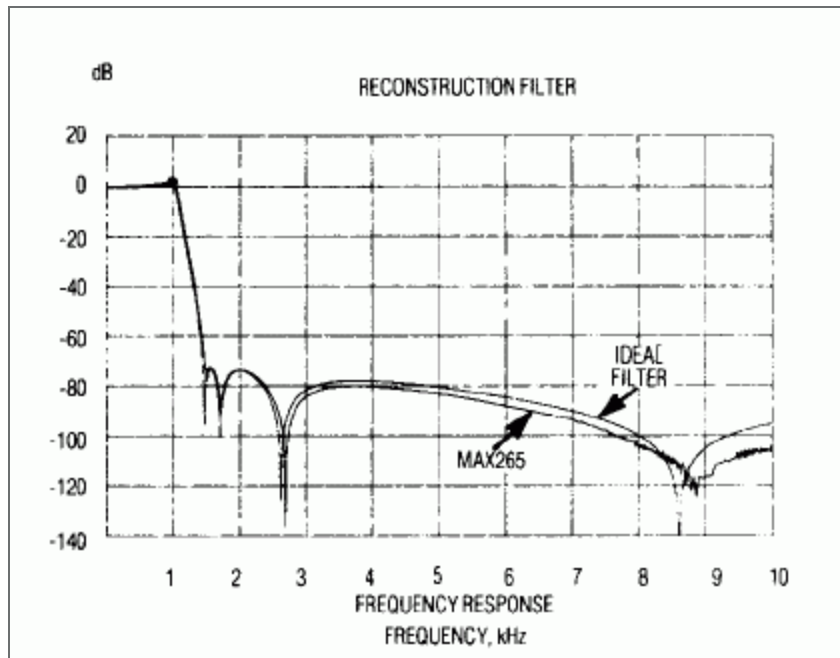


Figure 5. The circuit response of Figure 1 compares well with that of an ideal filter.

To assure maximum dynamic range, the four biquad-filter sections (two in each IC) exhibit increasing  $Q$  from input to output, The pole-zero pairs of each section also exhibit increasing frequency, which minimizes the spread in component values. The following pole and zero values produce a 1-rad/sec filter passband:

Table 2.

Section	$f_{\text{pole}}$ (Hz)	$Q_{\text{pole}}$	$f_{\text{Zero}}$ (Hz)
1	0.1005	0.5603	0.2397
2	0.1310	1.0540	0.2777
3	0.1564	2.3876	0.4273
4	0.1685	8.5145	1.4016

Note the feedback capacitors C1-C4 across each output op amp. These capacitors have two purposes; they improve the quality of transmission zeroes, and the form 1-pole lowpass filters that help to smooth out the discrete-level steps introduced by the filter's switched-capacitor action. The 1-pole filters have little effect on the passband shape because their high corner frequencies introduce only 0.1dB of loss at 1kHz.

Note also, that the applied clock frequency in Figure 2 (192kHz) allows use of a convenient binary-64 divider for setting the necessary 3X ratio between the converter's sample rate and the filter's 1kHz corner frequency,  $f_0$ . Each chip is programmed for an  $f_{CLK}/f_0$  ratio of 191.64 by V+ and V- connections to the filter inputs, F0-F5.

#### Related Parts

<a href="#">MAX265</a>	Resistor-Pin-Programmable, Universal Switched Capacitor Filter	<a href="#">Free Samples</a>
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#### More Information

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APPLICATION NOTE 29, AN29, AN 29, APP29, Appnote29, Appnote 29

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