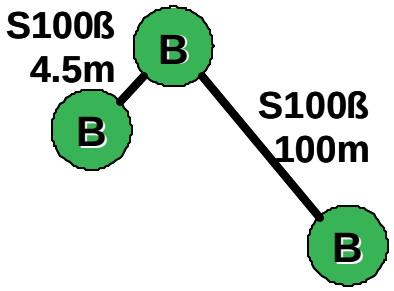
TSB41BA3 Errata

ERRATA ID	PROBLEM DESCRIPTION	RESOLUTION / WORK-AROUNDS
1. BOSS Arbitration Issue	Symptom A bus-reset may occur in certain topologies when 1394b BOSS arbitration is in use. Occurrences This issue is only possible if three or more BOSS-arbitration capable nodes are connected through a 1394b connection. To be BOSS-arbitration capable a node must have a 1394b PHY and a 1394b Link using the 1394b PHY-Link interface connection. If a narrow timing window is violated (dependent on cable lengths and/or mixed speed bus hops), then a middle node may detect a packet collision, causing a state-timeout. The state timeout causes a bus reset. Repetitive occurrences result in repetitive bus resets. Example Topologies A) Mixing short and long cable lengths. A BOSS arbitration issue may occur in the middle node:  	A. Use 1394a Link Layer Controllers. If the network only consists of nodes using 1394a Link Layers, then BOSS arbitration is not utilized; gap delays are maintained and therefore are not affected by this errata. B. In nodes that do not have a link, disable BOSS arbitration (e.g., force the BMODE pin to the logic 0 state).

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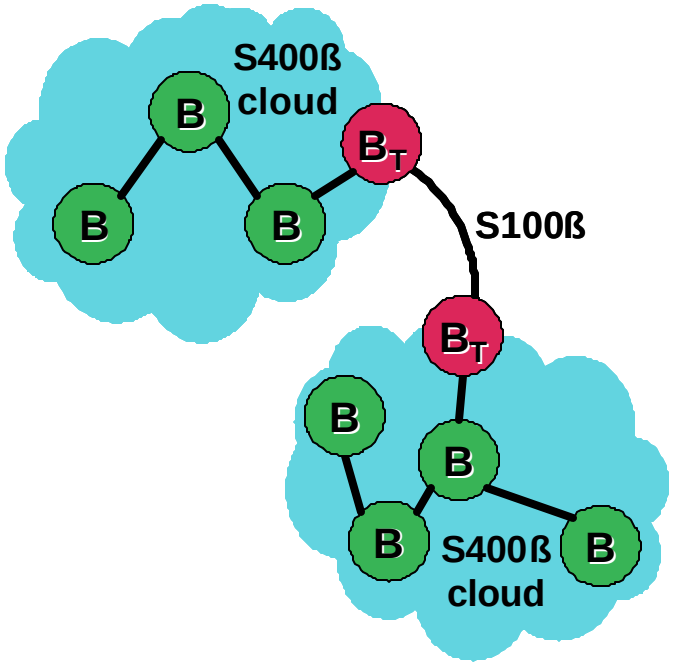
	B) Mixing bus hop speeds. Either transition node ("B_T") may have a BOSS arbitration issue:  <u>Detailed Example Situation</u> Refer to the diagram below. 1. Node #2 transmits a high-speed packet that ends an Async Subaction or the Isoch period. 2. Node #2 advances the Async phase (no requests pending for the current phase). 3. Node #0 has a bus request pending for the new phase. 4. Node #2 sends an Async grant.	

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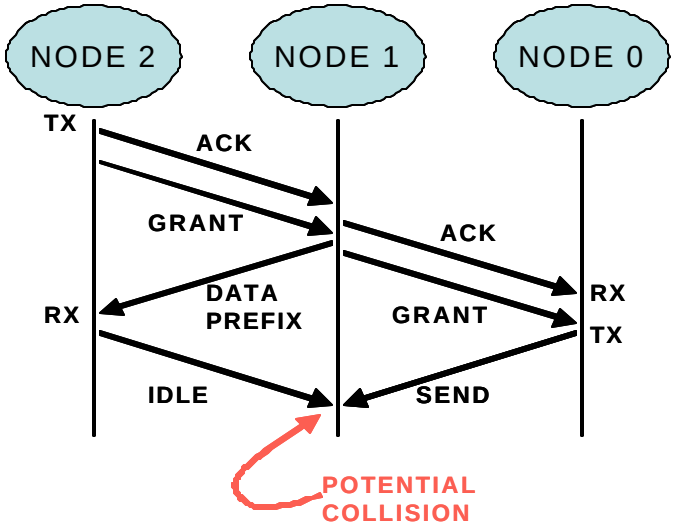
	5. The Async grant is forwarded through a senior node (Node #1) and down through a junior connection to Node #0. 6. If a narrow timing window is violated, then the middle node (Node #1) will detect a packet collision, causing a state-timeout while forwarding the grant to the next node. The state-timeout will cause a bus reset. 	
2. Missing Subaction Gap Issue	Symptom When nonroot 1394b nodes request transactions and do not receive an Ack (missing-Ack timeout occurs) the 1394b Link Layer is only sent an Arbitration Reset gap indicator rather than a both the Subaction gap and Arbitration Reset gap indicators. Some Link Layer controllers hang if the Subaction gap indicator is not received. Occurrences This does not occur with TI Link Layers and has only been observed by one other Link Layer manufacturer.	Instruct the Link Layer Controller to use 1394a mode for the PHY-Link interface.

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3. Cycle Start Concatenation Issue	Symptom When the PHY-Link interface is in the 1394a mode (BMODE terminal is logic 0) cycle start concatenation only works at S100. Furthermore, only one Isoch packet per Iso interval is allowed unless all Isoch packets are S100.	Configure the Link Layer Controller to only transmit one Isoch packet per Iso interval and do one (or both) of the following: A. Disable cycle-start packet concatenation in the Link-Layer Controller. B. Clear the EAA and EMC CFR register bits in the TSB41BA3. These bits are cleared by chip reset (default).
4. Incorrect PHY repeater delay.	Table 3 in the datasheet lists the PHY repeater *Delay* parameter as 144 + (delay x 20) ns and the *Delay* field as 0. The *Delay* field default is 4b'1111 (0xF) and not enough bits are available to accurately reflect the worst-case PHY repeater delay (5 bits are needed). The worst-case PHY repeater delay is 538 ns, 310 ns and 196 ns for S100, S200 and S400, respectively.	System designers may need to evaluate overall packet transfer time from worst-case nodes. Completely daisy-chained topologies at S100 may exceed the 1394a specified worst-case subaction gap timeout limit. Star or Hub approaches are usually within design timeout limits.
5. V_{OH} (min) not met at 3.3 V_{DD} (min)	The V_{OH} does not meet the minimum level specified (2.8 V) when the 3.3 V_{DD} supply is at minimum (3.0 V).	

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